



Attorney's Docket No. 42390.P3679C

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

David J. Sager

Examiner: Nasser G. Moazzami

Serial No.: 10/629,244

Art Unit: 2187

Filed: July 28, 2003

Customer No.: 008791

For: PROCESSOR AND DATA CACHE WITH DATA
STORAGE UNIT AND TAG HIT/MISS LOGIC
OPERATED AT FIRST AND SECOND
CLOCK FREQUENCIES

CONFIRMATION No.: 7585

MS: Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

TERMINAL DISCLAIMER UNDER 37 C.F.R. § 1.321(c)

The undersigned attorney represents that the undersigned attorney is the attorney of record for the above-referenced patent application.

The assignee of the entire right, title, and interest in and to the above-referenced patent application is Intel Corporation ("assignee"),

(Name of Assignee)

a Delaware corporation having a place of business at

(State of Incorporation)

2200 Mission College Blvd., Santa Clara, California 95052

(Address)

The terminal part of any patent granted on the above-identified application that would extend beyond the expiration of the full statutory term of

X United States Patent No. 6,631,454, entitled

Processor and data cache with data storage unit and tag hit/miss logic
operated at a first and second clock frequencies, and dated

October 7, 2003, as presently shortened

by any terminal disclaimer,

Application No.: 10/629,244

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Attorney Docket No.: 42P3679C

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X United States Patent No. 6,631,454,

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this agreement to run with any patent granted on the above-identified application and to
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No disclaimer is being made as to any terminal part of any patent granted on the
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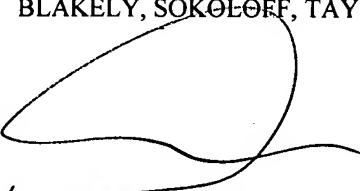
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Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: February 28, 2006



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